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10/544,787	05/26/2006	Pere Roca I Cabarrocas	0510-1120	8230

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EXAMINER	
WHALEN, DANIEL B	
ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

DocketingDept@young-thompson.com

Office Action Summary	Application No.	Applicant(s)	
	10/544,787	ROCA I CABARROCAS ET AL.	
	Examiner	Art Unit	
	DANIEL WHALEN	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,14-21 and 23-27* is/are pending in the application.

4a) Of the above claim(s) *1-10,20 and 21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11,14-19 and 23-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "forming an insulator on top of said active material and electrodes" in **claim 11** and "a top gate transistor" in **claim 18** and "the substrate...is patterned to form source and drain electrodes" in **claim 19 must** be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. In response to the amended claims to overcome the claim objections, the amended claims do not completely overcome the claim objections and there are still numerous errors remaining as set fourth in this office action. Appropriate correction is required.

Claim 11 is objected to because of the following informalities: "a microcrystalline film" in line 10 should be read -- a microcrystalline silicon film -- in order to be consistent with “said microcrystalline silicon film” recited in line 15. “plasma treated interface” in line 20 should be read -- said plasma treated interface --. “element wherein” in line 13 should be read -- element, wherein --. Lastly, in order to clearly recite the claimed subject matter, as a suggestion, the recitation in lines 5-11 should be read -- deposition method; forming an insulator on top of said active material and electrodes; forming a plasma treated interface on top of said insulator; and forming a microcrystalline silicon film on top of said treated interface at a temperature between 100ºC and --.

Claims 15-17, 24 are objected to because of the following informalities: “elements is” in line 3 of claim 15 should be read -- element is --. “elements are” in line 3 of claim 16 should be read -- element is – to be consistent with claim 11 reciting “a deposition chemical element”. “elements generate” in lines 3-4 of claim 17 should be

read -- element generates --. "The a method" in line 1 of claim 24 should be read -- The method --.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 11, 14-19, and 23-27** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. For instance, the recitation of "forming an insulator on top of said active material and electrodes" in claim 11 was not described in the specification (see fig. 1 & page 5, lines 16-35). Instead, it appears from the specification that the insulator is formed above the gate electrode formed on the substrate. Claims 14-19 and 23-27, which depend from claim 11, are rejected.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 17 and 19** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. **Re claim 17**, the recitation of "generate a flux" is unclear what would be considered as "a flux". Is it referring to a flow rate?

8. **Re claim 19**, the recitation of "substrate…is patterned to form source and drain electrodes" is unclear since the TFT structure discussed in the specification is either top or bottom gate transistors formed on the substrate, wherein the substrate is not patterned to form source and drain electrodes.

Insofar as definite, and as best understood, the claims are rejected as follows.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 11, 14-19, and 23-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakata et al. (US 6,078,059; hereinafter "Nakata") in view of Roca et al. ("Stable microcrystalline silicon thin-film transistors produced by the layer-by-layer technique"; hereinafter "Roca") and Yoshinouchi et al. (US 5,403,756; hereinafter "Yoshinouchi").

11. **Re Claim 11,** Nakata teaches a method for producing a transistor for active matrix display comprising the steps of:

forming an active material and electrodes (12 with active material Ta) on a substrate (11), said active material being formed using a vapor deposition method (sputtering); and

forming an insulator (14) on top of said active material and electrodes, wherein,

a plasma treated interface (top surface of 14) is formed on top of said insulator,

a microcrystalline film (15) is formed on top of said treated interface at a temperature comprised between 100 and 400ºC (300ºC) using at least a deposition chemical element (SiH_4) and a crystallization chemical element (H_2) (col. 9, lines 3-16).

said plasma treated interface is selected from the group consisting of a SiN_x layer, a SiN_xO_y layer, a SiO_2 layer and glass (col. 8, lines 61-67, Si_3N_4), and

plasma treated interface using a gas selected from the group consisting of N_2, O_2, N_2O and NH_3 (col. 8, lines 61-67, NH_3).

Although Nakata does not explicitly disclose more than one active material and electrode, it would have been obvious to one of ordinary skill in the art that the more than a single transistor would be formed in the semiconductor manufacturing process in order to provide high density integrated circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form more than one active material and electrode in order to provide the high density integrated circuits.

However, Nakata does not explicitly disclose that the crystalline fraction is above 80% and that the microcrystalline silicon film comprises grains of a size between 10nm

and 400nm. Regarding the crystalline fraction, Roca teaches forming a microcrystalline film, wherein the crystalline fraction being above 80% so as to obtain stable film (Abstract & Introduction). Regarding the grain size, one of ordinary skill in the art would easily recognize that the microcrystalline film is a film that formed of small grains as evidenced by Yoshinouchi teaching that the microcrystalline silicon film comprises grains of a size between 10nm and 400 nm (col. 11, lines 37-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Nakata with that of Roca so as to obtain stable microcrystalline film and with that of Yoshinouchi so to form the microcrystalline film.

Re Claim 14, although the combined teaching of Nakata, Roca, and Yoshinouchi does not explicitly disclose using a buffer gas selected from the group consisting of Ar, Xe, Kr, and He for forming the microcrystalline film, one of ordinary skilled in the art would recognize that the buffer gas selected from the group consisting of Ar, Xe, Kr, and He is used as a carrier/purging gas during CVD process. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the buffer gas selected from the group consisting of Ar, Xe, Kr, and He is used as a carrier/purging gas during CVD process.

Re Claim 15, Nakata teaches wherein said crystallization chemical elements is H_2 (col. 9, lines 3-16).

Re Claim 16, Nakata teaches wherein said deposition chemical elements are selected among the group comprising SiH_4 and SiF_4 (col. 9, lines 3-16).

Re Claim 17, although the combined teaching of Nakata, Roca, and Yoshinouchi does not explicitly disclose that said deposition chemical elements generate a flux and said crystallization chemical elements generate a flux, both of which are at equilibrium during the growth of the microcrystalline silicon film, one of ordinary skill in the art would readily adjust the parameter during CVD deposition process to obtain optimized microcrystalline film. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the deposition chemical elements flux and the crystallization chemical elements flux are at equilibrium during the growth of the microcrystalline silicon film so as to obtain optimized microcrystalline film.

It is noted that Examiner interpreted the "a flux" to be gas containing either the deposition chemical element or the crystallization chemical element inside the chamber during the step of forming the microcrystalline silicon film.

Re Claim 18, Yoshinouchi teaches wherein a top gate transistor is formed (fig. 9B).

Re Claim 19, Nakata teaches wherein the substrate comprising a metallic layer (Ti) is patterned to form source and drain electrodes (col. 9, lines 28-32).

It is noted that Examiner interpreted the recitation of "substrate comprising a metallic layer is patterned to form source and drain electrodes" as the layer comprising the metallic layer is patterned to form source and drain electrodes.

Re Claim 23, although the combined teaching of Nakata, Roca, and Yoshinouchi does not teaches a thickness of the microcrystalline silicon film between 100 nm and 450 nm, it has held that discovering an optimum or workable ranges involves only

routine skill in the art. *In re Aller*, 105 USPQ 233. Furthermore, if the only difference between the prior art and the claims is a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not performed different than the prior art device, the claimed device is not patentable distinct from the prior art device: *In re Gardner v. TEC Systems, Inc.*, 220 USPQ 777.

Re Claim 24, although the combined teaching of Nakata, Roca, and Yoshinouchi does not explicitly disclose that the microcrystalline silicon film is produced by a hot wire technique, it is conventionally known to one of ordinary skill in the art that the hot wire CVD method is a readily known CVD types that deposits amorphous or microcrystalline silicon in silicon based TFT. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the microcrystalline film is formed by a readily available HWCVD so as to form the predictable silicon layer in the TFT.

Re Claim 25, Nakata teaches wherein the microcrystalline silicon film is produced by a radiofrequency glow discharge technique (RF-PCVD).

Re Claim 26, similar to argument in claim 24, although the combined teaching of Nakata, Roca, and Yoshinouchi does not explicitly disclose that the vapor deposition methods use a radiofrequency glow discharge technique, it is conventionally known to one of ordinary skill in the art that the RF-PCVD method is a readily known CVD types in silicon based TFT. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the vapor deposition methods use radiofrequency glow discharge technique so as to form the predictable active material layer in the TFT.

Re Claim 27, although the combined teaching of Nakata, Roca, and Yoshinouchi does not explicitly disclose that the vapor deposition method uses a 13.56 MHz, one of ordinary skill in the art would recognize that the frequency, 13.56 MHz, is the standard radio frequency of the plasma CVD process.

Response to Arguments

12. Applicant's arguments with respect to amended claims have been considered but are moot in view of the new ground(s) of rejection. Furthermore, in response to applicant's argument (page 10) that both top and bottom gate transistors are illustrated by fig 1, it is not convincing since fig. 1 is clearly limited to the bottom gate transistor. Furthermore, the specification discloses that fig. 1 is a schematic view of a TFT structure for a bottom gate transistor (see page 5, lines 1-2). Therefore, the drawing objection is maintained. Furthermore, new drawing objections are raised to due to amended claims filed on 03/02/2010.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL WHALEN whose telephone number is (571)270-3418. The examiner can normally be reached on Monday-Friday, 7:30am to 5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. W./
Examiner, Art Unit 2829
03/29/2010

Daniel Whalen
/Michael S. Lebentritt/

Primary Examiner, Art Unit 2829